X-Band MMIC Amplifier with Pulse-Doped GaAs MESFET's

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Abstract—**An X-band monolithic four-stage low noise amplifier (LNA) with 0.5 μm-gate pulse-doped GaAs MESFET's was successfully demonstrated for a direct broadcast satellite (DBS) converter. This paper presents the design and the test results. The key feature of the research is a detailed demonstration of the advantages of using series feedback with experiments and simulations. This LNA shows an excellent input VSWR match of under 1.3 and an output VSWR match of under 1.4 as well as a noise figure of 1.67 dB and a gain of 24 dB at 12 GHz. Moreover, the noise figure, the gain and VSWR's exhibit very little bias current dependence due to the exceptional features of the pulse-doped structure FET's and the optimized circuit design. Insensitivity to bias current implies performance stability in the face of process fluctuations. Thus, the yield of chips with noise figures of less than 2.0 dB is as high as 62.5%, and the variations of gain and VSWR are highly uniform as well.**

I. Introduction

SINCE Japanese DBS began in 1984, households receiving DBS have been increasing, and the number has already risen above four million in Japan. Monolithic microwave integrated circuits (MMIC's) have been developed principally for non-commercial applications such as phased-array radars and electronic warfare systems. R&D of consumer-adaptable MMIC's such as in DBS converters is becoming vigorous today, owing to recent advances in GaAs materials and processing [1], [2]. The merits of monolithic integration are miniaturization, reduction of assembly cost and improvement of reliability.

Some laboratories have reported on an ion implantation approach for MMIC's because of excellent uniformity and reproducibility of device characteristics [3]–[6]. It is, however, difficult for ion-implanted MESFET's to suppress the short channel effect because a two-dimensional field distribution effect appears in their active layers (about 1000 Å thick) [7]. Therefore, device performance cannot be significantly improved at sub-micron gate lengths.

AlGaAs/GaAs high electron mobility transistors (HEMT's) are the most popular device in microwave application today, because of their excellent low noise and high gain performance. Pseudomorphic HEMT's and InP-based HEMT's have shown superior performance up to the millimeter-wave region [8]–[12]. It is, however, our view that a HEMT-based technology is not necessarily a unique solution for monolithic microwave LNA's. In the case of HEMT-based MMIC's, extremely refined epitaxial technology is required, because the critical control of layer thickness, doping concentration and abruptness at the heterointerface dominates the device performance.

The objective of this work is to develop a cost-effective and mass-producible LNA with high performance for consumer application using relatively simple technology. GaAs MESFET's with highly doped, very narrow active regions, known as pulse-doped MESFET's, are applied for this purpose. Epitaxial technology is used for the very narrow active regions, because it has the advantage of controllability of the carrier profile, which strongly affects the device characteristics. Pulse-doped MESFET's are less difficult than HEMT's from the standpoint of productivity because of their simple structure. Excellent low noise characteristics comparable to AlGaAs/GaAs HEMT's with the same dimensions and high uniformity were reported, and an MMIC amplifier has also been demonstrated in previous works [13]–[15].

One of the specific features of this LNA is the excellent low input VSWR with high uniformity. For high volume consumer application such as DBS receivers, total system cost including assembly cost as well as chip cost is the most important problem. Troublesome cutting and pasting to tune the matching circuit outside of this LNA should be eliminated from the assembling process of DBS converters to ensure low assembly cost. Therefore, this LNA was designed with special attention to improvement of the input VSWR and the yield as well as reduction of the noise figure.

This paper presents the design and RF results. The key to the design of an LNA is to optimize series feedback inductance [16]. The relation between basic FET parameters and series feedback inductance, which is very important for a circuit design, was examined in detail with measurement and simulation for the first time. In the following discussion, the circuit design procedure based on this basic examination, the performance of LNA's and their distribution are described.

Manuscript received April 4, 1991; revised August 5, 1991.

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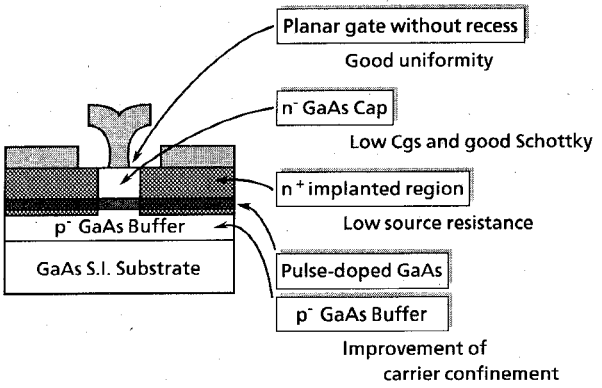


Fig. 1. Structure and features of pulse-doped GaAs MESFET.

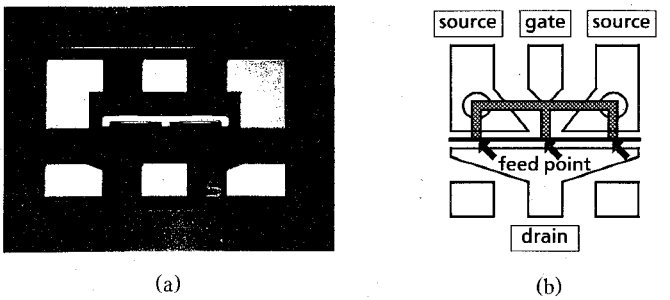


Fig. 2. Basic configuration of each FET used in amplifier. (a) SEM photograph. (b) Layout pattern.

II. Device Technology and DC Characteristics

Fig. 1 shows the structure and the features of a pulse-doped GaAs MESFET. A planar structure is one of the most important factors for MMIC application to improve the uniformity and reproducibility of FET characteristics. To fabricate this structure, an undoped p^- GaAs buffer layer (1 μm), a Si-doped GaAs active layer ($4\times10^{18}/cm^3$, 100 Å), and an undoped n^- layer (300 Å) were successively grown by OMVPE on a semi-insulating GaAs substrate. The undoped p^- and n^- layers are formed by simply controlling the V/III ratio of source materials. The active areas were isolated by mesa etching. The submicron gates were defined using conventional photolithography techniques based on T-shaped dummy gate self-alignment [13], [14]. A T-shaped resist mask with a 0.2 μm undercut was formed by anisotropic RIE. The n^+ regions were formed by the self-align implantation of Si ions. Ohmic contacts were formed by evaporating Ni/AuGe and successively alloying at 450°C. Gate metals of Ti/Pt/Au were substituted for the dummy gate. The gate length was 0.5 μm, the length of the top of the gate metal was 1.2 μm and source/drain electrode spacing was 4.0 μm.

Monolithic integration was realized using via-holes for grounding, metal-insulator-metal (MIM) capacitors employing 3000 Å thick silicon oxi-nitride, and airbridges for gate-feed circuits, etc. The substrate thickness was 100 μm.

The typical dc characteristics of these devices are an Idss ($Vg = 0$ V, $Vd = 2$ V) of 204 mA/mm with a pinch-off voltage of -1.0 V and a maximum transconductance of 320 mS/mm.

III. Decision on Unit FET for LNA

Each FET used in the amplifier has a gate width (Wg) of 280 μm with a three gate-feed configuration, as shown in Fig. 2. Two experiments were carried out in order to decide on the shape and size of the unit FET.

First, four kinds of FET's with one, two, three, and five gate-feed points were actually made and measured to examine the optimum number of gate-feed points for low noise. As it is unrealistic to make a lot of these test element groups (TEG's) for every possible gate width, these experiments were made with FET's 280 μm wide, a size often used for X-band application. The measurement results showed that the three gate-feed configuration achieved the best minimum noise figure value (Fmin) at 12 GHz. Fmin increases with gate resistance (Rg) and gate capacitance (Cgs) as the following Fukui's equation suggests:

$$\mathrm{Fmin} = 1 + 2\pi f\,\mathrm{Cgs}\,K_f\sqrt{\left(\frac{Rg + Rs}{gm}\right)} \qquad (1)$$

K_f fitting factor
f frequency
Cgs gate capacitance
Rg gate resistance
Rs source resistance
gm transconductance.

As the number of gate-feed points (Ngfp) becomes higher, the gate resistance decreases but the parasitics of gate capacitance in the gate-feed circuits increases. Hence the Ngfp has the optimum value for the lowest Fmin.

Secondly, it must be confirmed that the Wg of 280 μm is optimum. The measurement was made by using a TEG which includes five kinds of FET's of 160 μm, 200 μm, 240 μm, 280 μm and 320 μm gate widths with three gate-feed points. The measurement results indicated that the 240 μm ~ 280 μm FET gave minimum Fmin and that the equivalent noise resistance (Rn) directly decreased with the gate width. The source resistance (Rs) decreases and the Rg increases with Wg. It is obvious from Fukui's equation that a FET of low Rs and low Rg has low Fmin. Therefore, the Wg of 280 μm was decided upon from the standpoint of minimum Fmin and low Rn.

Thus, the shape and size of a unit FET for an LNA was decided upon. Fig. 3 illustrates measured Fmin and associated gains (Ga) versus drain current for 0.5 μm$\times$280 μm FET's with three gate-feed points at 12 GHz. A minimum Fmin of 1.23 dB with associated gains of 9.0 dB was measured at 12 GHz and was relatively independent of drain current. These superior features make it possible to design low noise amplifiers with a large margin for bias

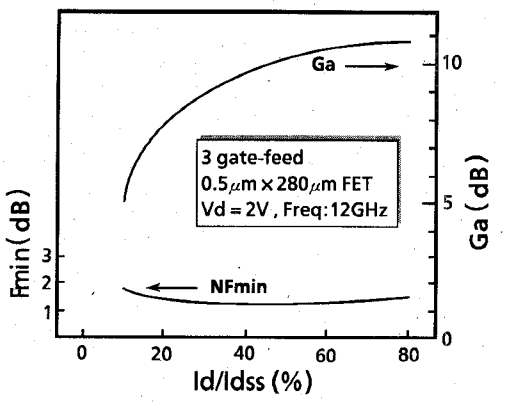


Fig. 3. Measured Fmin and Ga versus Id.

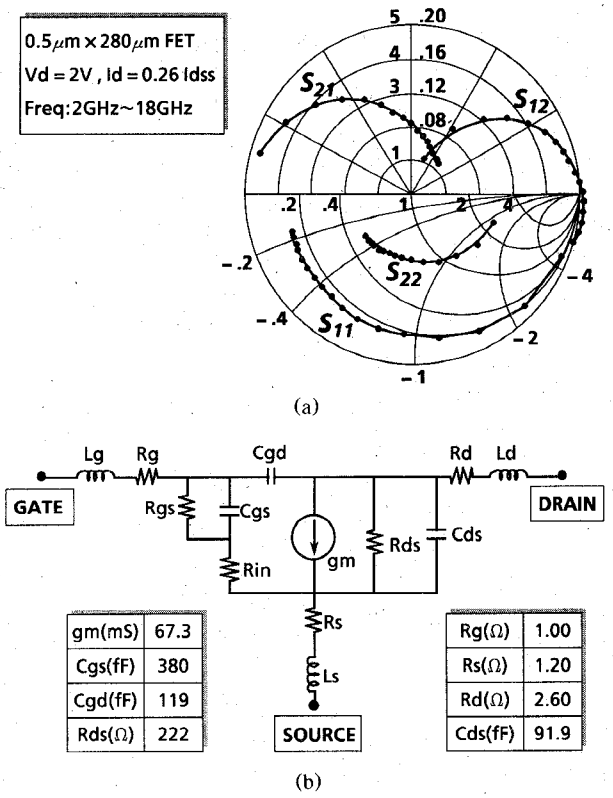


Fig. 4. Measured *S*-parameters and small signal model at the lowest noise condition. (a) Measured *S*-parameters. (b) Small signal model.

conditions, and are due to the excellent carrier confinement of this pulse-doped structure [17].

Fig. 4 shows measured *S*-parameters up to 18 GHz of a FET at the lowest noise condition ($Vd = 2$ V, $Id = 0.26$ Idss) and a small signal model. The small signal model shown in Fig. 4(b) was obtained by fitting to measured *S*-parameters. The transconductance was estimated to be 67.3 mS (240 mS/mm) at this bias condition.

IV. Relation Between FET Parameters and Series Feedback Inductance

There are two serious design problems for an LNA. First, it is difficult to achieve simultaneous noise match and input VSWR match because the optimum source

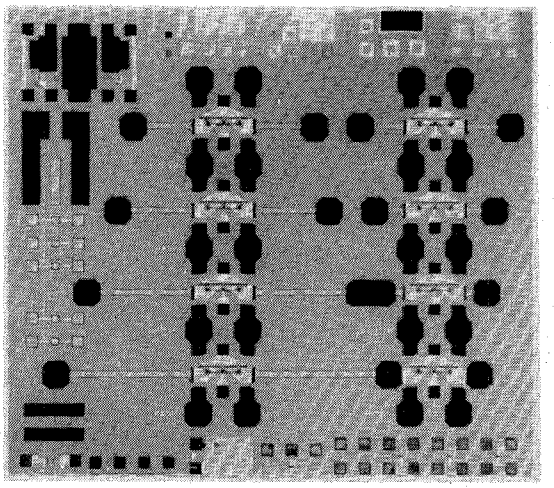
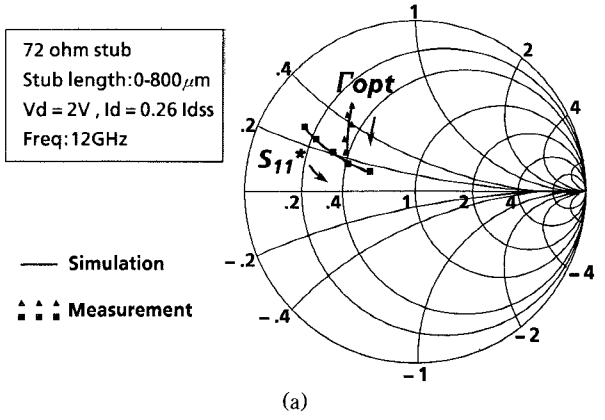


Fig. 5. Photomicrograph of TEGs to measure FET parameters versus series feedback inductance.

reflection coefficient (Γopt) is not simply the complex conjugate of the input reflection coefficient (S_{11}^*). Secondly, it is impossible to realize simultaneous input and output VSWR matches because the Rollett's stability factor (K) of low noise devices tends to be smaller than 1.0. In fact, the stability factor K of a 0.5 μm×280 μm pulse-doped MESFET to be adapted to the LNA was 0.48 at 12 GHz. A series feedback inductance settles these two problems and the design of LNA's usually involves the use of series inductive feedback elements [16]. This is a well-known technique but detailed examination of the relation between FET parameters and series feedback inductance has not been extensively reported. Therefore the correlations between series feedback inductance (i.e., the length of source stub) and parameters of the pulse-doped MESFET's were examined using experiments and simulations in order to find the value of the optimum feedback inductance. The purpose of the experiments was to verify the accuracy of the simulations. The experiments were made using actual TEG's as shown in Fig. 5. Each FET has source stubs of 72 Ω impedance, ranging in length from 50 μm to 800 μm. Taking topological symmetry into consideration, two source stubs are formed symmetrically as shown in Fig. 5, to prevent partial current flow from a drain to a source. The equivalent circuit of each FET has the parallel connection of the same stubs.

The relation of some FET parameters to the stub length (lst) is more immediate and more convenient for circuit design and layout design than their relation to the series feedback inductance values. An inductance value of just one stub 100 μm long (72 Ω impedance) is equivalent to 68 pH at 12 GHz and therefore a parallel connection of two 100 μm stubs has an inductance of 34 pH. In the following discussion, a certain stub of lst means this parallel connection of two stubs of lst. The measurements and simulations were made at the bias condition of $Vd = 2$ V and $Id = 0.26$ Idss.

Fig. 6(a) shows how Γopt and S_{11}^* change on a Smith chart with stub length. The solid lines are simulation



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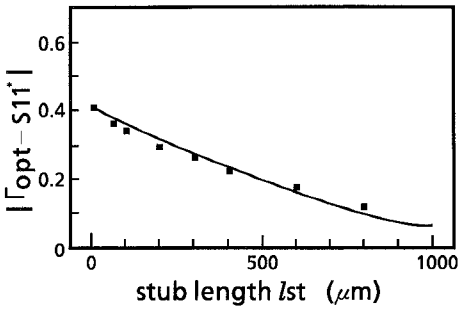


(b)

Fig. 6. Change of Γopt and S_{11}^* with stub length. (a) Change of Γopt and S_{11}^* on Smith chart with stub length. (b) $|\Gamma opt - S_{11}^*|$ versus stub length.

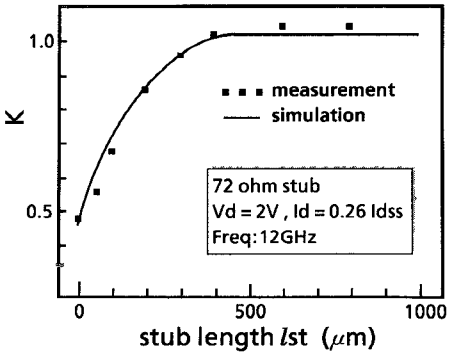


Fig. 7. Rollett's stability factor (K) versus stub length.

results and the dots are measurement data. They approach each other with increasing lst. Fig. 6(b) illustrates the same kind of plot but this is $|\Gamma opt - S_{11}^*|$ versus lst. It can be seen that the difference between Γopt and S_{11}^* decreases almost linearly with lst. According to these figures, the longer stub results in lower input VSWR up to 1000 μm when matching networks are synthesized so that the amplifier has the minimum noise figure. This is important information especially for the design of the first stage of an LNA.

Fig. 7 shows Rollett's stability factor (K) versus lst. The K goes up with lst at 12 GHz as shown here. A stub length of 400 μm seems to be long enough for the K to reach 1.0, because a FET with a K of more than 1.0 is

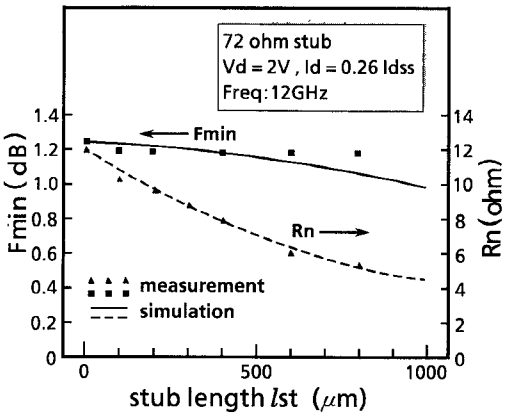


Fig. 8. Fmin and Rn versus stub length.

unconditionally stable. It is, however, expected that operation stability is susceptible to process fluctuations because the gradient of K to lst is relatively steep around 400 μm. This figure suggests that it is better to choose stubs somewhat longer than 400 μm, i.e., more than 500 μm, from the standpoint of the production yield.

Fig. 8 shows Fmin and Rn versus lst. Measured Fmin has little dependence on lst as shown in Fig. 8. According to the simulation results, Fmin slightly decreases with a longer stub, which can be explained as follows. A lossless feedback element will not affect the minimum noise measure (Mmin) [16]. Increasing series feedback inductance reduces the available gain (Gav); therefore Fmin diminishes accordingly, as shown in the following equation:

$$\text{Mmin} = \frac{\text{Fmin} - 1}{1 - 1/\text{Gav}} \approx (\text{Fmin} - 1)(1 + 1/\text{Gav}) \quad (2)$$

The difference between the measurement and the simulation in Fig. 8 is within the limits of measurement errors. Therefore we can consider that stub length produces very little effect on the noise figure.

Rn is important for the prediction of the variation of noise figures. The smaller the Rn, the more variation tolerance, because constant noise contours have greater separation and are larger in diameter for a given Fmin. Rn decreases with longer lst and tends to slightly saturate at over 600 μm.

V. Circuit Design

The principal aim of the design is to attain not only a low noise figure but also good VSWR matches with high uniformity so that the LNA can be employed without any impedance tuning outside the IC. The key to the design is to optimize series feedback inductance. The above-mentioned examination makes it clear that a more than 500 μm stub is required from the standpoint of K, and that a longer stub generally gives better results for the other parameters which are important for the design of an LNA.

The design goal was a noise figure of less than 2.0 dB, a gain of 24 dB and VSWR matches of under 2.0. Based on

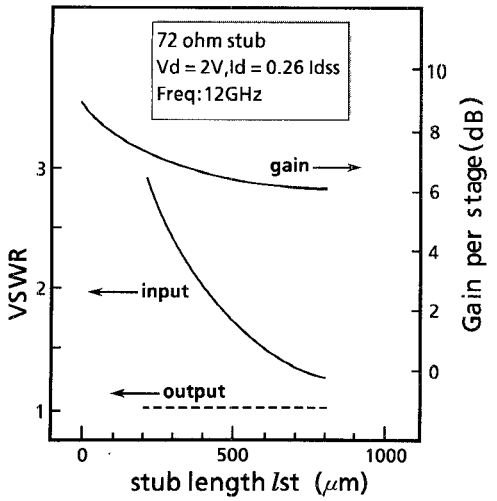


Fig. 9. Gains and VSWR matches versus stub length for noise match.

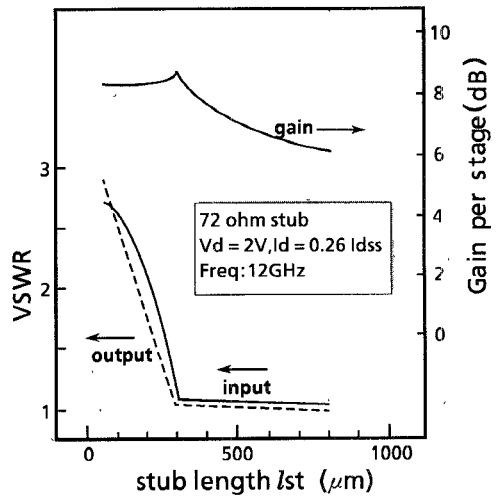


Fig. 10. Gains and VSWR matches versus stub length for gain match.

the fundamental considerations described above, performances of an amplifier per stage were simulated by varying *l*st.

Fig. 9 illustrates simulation results of gains and VSWR matches where the matching networks are synthesized so that an amplifier per stage has the minimum noise figure (i.e., noise match). The first stage should generally be designed with noise match because it determines the overall noise figure. As the stub length must be more than 500 μm as mentioned before, an input VSWR of under 1.5 can be achieved as shown in Fig. 9. Accordingly, the input VSWR is surely within the design goal even if the fluctuation of *S*-parameters of FET's is taken into account. When the stub length of the first stage is set at more than 500 μm, it can be seen in Fig. 9 that the gain of the first stage is less than 6.4 dB.

Fig. 10 illustrates simulation results of gains and VSWR matches in which the matching networks are synthesized so that an amplifier per stage has the maximum gain and has the lowest VSWR's (i.e., gain match). When the stub

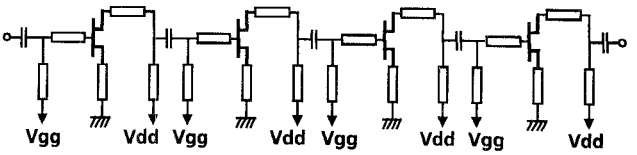


Fig. 11. Equivalent circuit of monolithic LNA.

length of the first stage is decided upon, Fig. 10 suggests how many stages are needed to obtain the overall gain of the design goal. The following stages are generally designed as gain match, because the noise figure of the first stage is dominant for the total noise figure. In the case of a three-stage amplifier, a gain of 8.8 dB per stage is needed in the following stages but Fig. 10 illustrates that this is impossible. On the other hand, input and output VSWR matches for gain match abruptly change at a 300 μm long stub as shown in Fig. 10. This means that the stub length of the gain match amplifier should be more than 400 μm (taking a little margin into consideration) with regard to VSWR matches.

Thus, an amplifier which meets the design goal must have a four-stage configuration. In the case of a four-stage amplifier, the required average gain per stage is 6 dB and Figs. 9 and 10 show that stub lengths of up to 800 μm can be selected for both noise match and gain match. From the above-mentioned study, 700 μm was decided upon for the length of the stubs of all the stages, considering a gain margin. The equivalent circuit of the monolithic LNA is seen in Fig. 11. Each source stub means a parallel connection of two stubs. The matching networks are designed employing 57 Ω transmission lines and 72 Ω transmission lines for the source stubs. Each stage has the same configuration as the first stage, because there is no difference of gains between a noise-matched amplifier and a gain-matched amplifier for a 700 μm long stub and because VSWR's are low enough for cascade connection.

Finally, the amplifier gain flatness across a frequency band should be examined. The frequency band of the DBS in Japan is 11.7 GHz to 12 GHz. The Electronics and Industries Association of Japan (EIAJ) recommends that the variation of conversion gain across the frequency band should be less than 4 dB. As the simulation results of the amplifier per stage suggested that the noise matched amplifier has a gain slope of -0.75 dB/GHz, the four-stage amplifier has a gain slope of -3 dB/GHz. Therefore, this amplifier has a sufficient frequency flatness of as low as 0.9 dB across the frequency band of interest, because it is easy to keep the total gain slope (including the following mixer and IF amplifier) at less than 4 dB in the frequency range between 11.7 GHz and 12 GHz.

VI. Results

A photomicrograph of the monolithic LNA is shown in Fig. 12. The chip size is 2 mm $\times$ 4.5 mm. Fig. 13 shows the frequency characteristics of LNA performances which were measured at the bias condition for the lowest noise

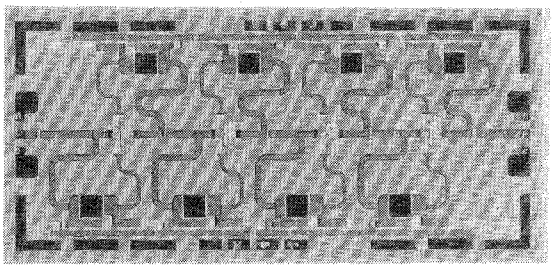


Fig. 12. Photomicrograph of monolithic LNA.

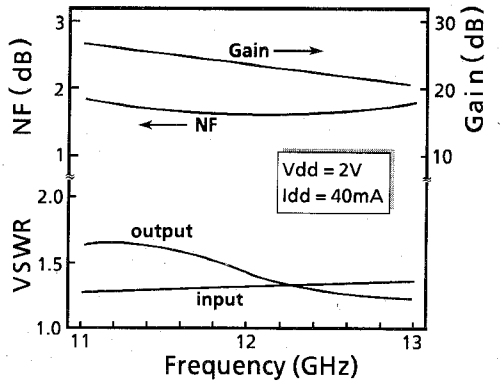


Fig. 13. Frequency characteristics of LNA performances.

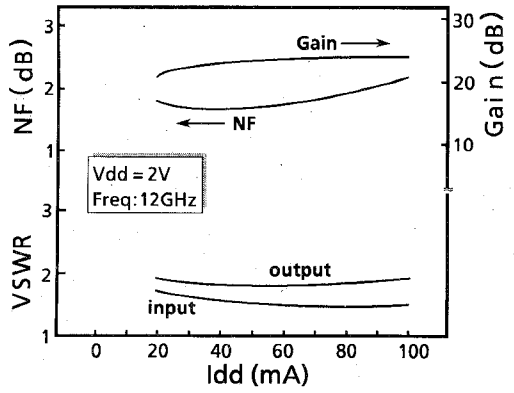


Fig. 14. Current dependence of LNA performances.

figure. They show a very good input VSWR match of 1.3 and an output VSWR match of 1.4, as well as a noise figure of 1.67 dB and a gain of 24 dB at 12 GHz as the design goal. This amplifier has a frequency flatness of 0.9 dB across the frequency band of interest as the simulation results suggested. Fig. 14 illustrates current dependence of LNA performances which were measured by controlling the gate bias voltage. It can be seen that the noise figure, the gain, and VSWR matches change little in the range between 20 mA and 80 mA. As a little variation of threshold voltages of FET's is inevitable because of process fluctuation, the operative condition of LNA's necessarily varies with each chip. Such insensitivity to current means that the performance is resistant to process fluctuation, and a high yield can be expected.

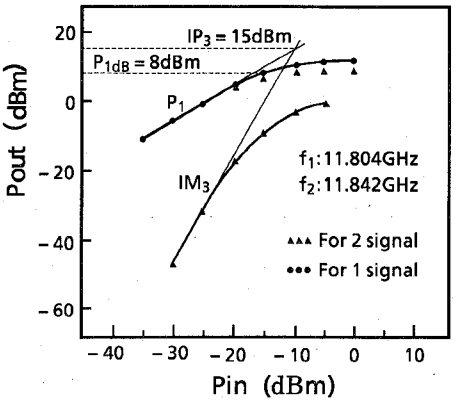


Fig. 15. Output power of the fundamental and IM_3 versus input power.

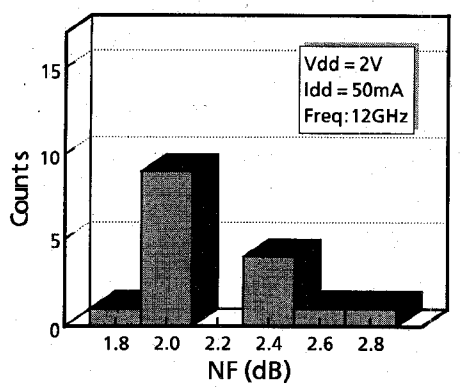
These characteristics are due to the excellent carrier confinement of the pulse-doped channel of this device.

Fig. 15 shows the output power (Pout) of the fundamental (P_1) and third-order intermodulation (IM_3) products versus input power. The frequencies of the two signals employed for the IM_3 measurement were 11.804 GHz and 11.842 GHz. It can be seen that the 1 dB compression point ($P_{1\ dB}$) is 8 dBm and that the third-order intercept point (IP_3) is 15 dBm. As the input power of this LNA is -80 dBm to -50 dBm for DBS application, the linearity performance is high enough.

Fig. 16 shows the distribution of the LNA performances which are from two 2-inch diameter wafers of the same lot. All chips were measured at the same power supply and the same bias condition without any impedance tuning. The number of LNA chips obtained from a 2-inch diameter wafer is relatively small because a multi-project mask set was employed and included a couple of circuits in addition to this LNA. The noise figures of 62.5% of the working chips are within 2.0 dB, and the input and output VSWR matches of 93.8% are under 1.4. The median of the gain distribution is somewhat lower than the design goal of 24 dB, but the gains of 75% of the chips are over 22 dB and the uniformity is excellent. This is because the 700 μm source stub designed was somewhat longer than the real optimum value and therefore the impedance margin was somewhat larger than the gain margin. The yield described here means what is called "intrinsic" yield, i.e., the fraction of chips that are within microwave specification relative to the number of chips that have been successfully fabricated without "mechanical" failures, as shown below [18]:

$$\text{intrinsic yield} = \frac{\text{chips within microwave specification}}{\text{chips that are dc functional}}$$

The percentage of chips which simultaneously meet the following conditions, noise figures of less than 2.0 dB, gains of more than 22 dB and VSWR's of under 1.4, is as high as 62.5% and very high uniformity is achieved.



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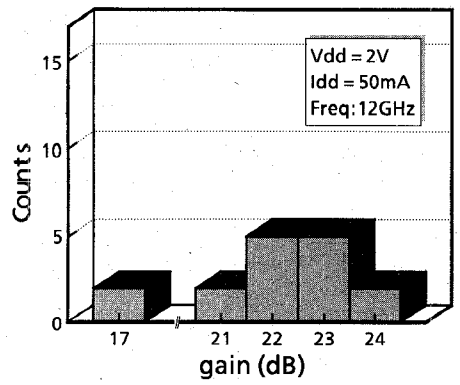

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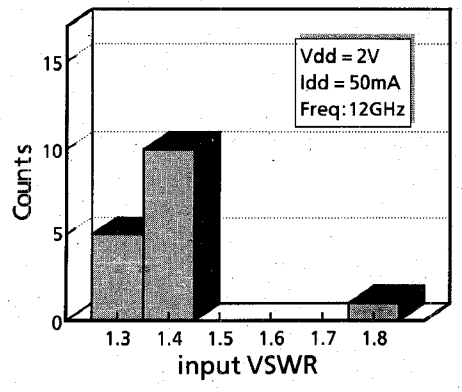

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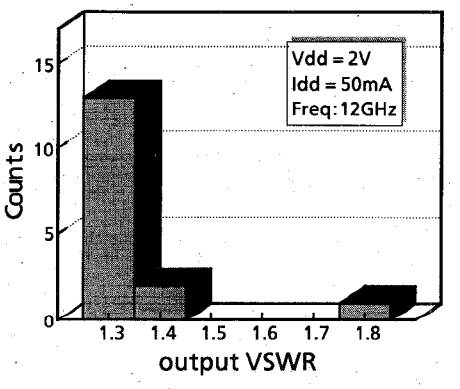

(d)

Fig. 16. Distribution of monolithic LNA performances. (a) Distribution of NF's. (b) Distribution of gains. (c) Distribution of input VSWR's. (d) Distribution of output VSWR's.

VII. Conclusion

An *X*-band MMIC amplifier with pulse-doped GaAs MESFET's has been demonstrated. It exhibits very good VSWR matches of under 1.4 as well as a noise figure of 1.67 dB and a gain of 24 dB at 12 GHz, which successfully meets the design goal. Moreover, the intrinsic yield within noise figures of 2.0 dB is as high as 62.5%, and the percentage of chips which simultaneously meet the following conditions, noise figures of less than 2.0 dB, gains of more than 22 dB and VSWR's of under 1.4, is as high as 62.5% and very high uniformity is achieved. In the assembling process of DBS converters, the input matching network is usually tuned by cutting and pasting strip lines in order to optimize their noise figure. This LNA makes it completely unnecessary to tune anything due to the excellent low input VSWR with high uniformity. The results of this monolithic LNA demonstrate that the MMIC technology based on pulse-doped MESFET's is quite promising for consumer application.

Acknowledgment

The authors would like to thank K. Nakayama, Y . Kai, K. Kawahara, K. Mukai, Y. Kawabata, and S. Aoki for their technical assistance. Special thanks are due to S. Shikata, Y. Hasegawa, T. Katsuyama, and M. Nishiguchi for their kind support. The authors are grateful to K. Yoshida, M. Koyama, H. Kotani, A. Ishida, and K. Koe for their encouragement and support.

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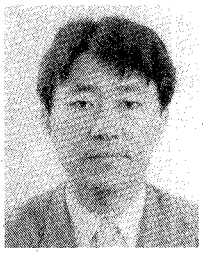

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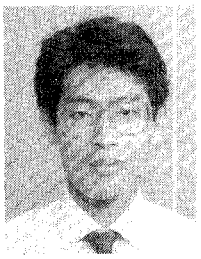

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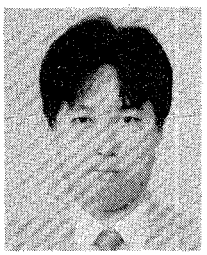

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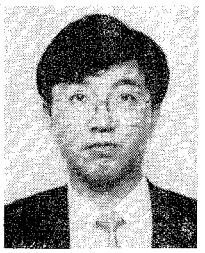

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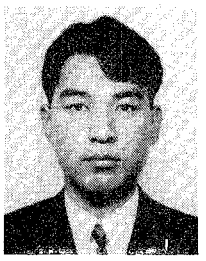

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